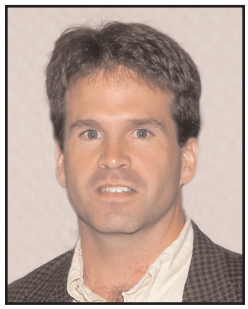
SE5 CMOS RF Design in 90nm and Beyond



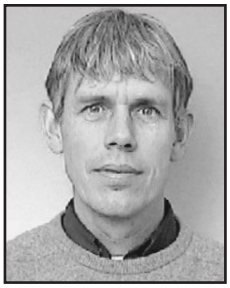
Organizer: David Su, Atheros Communications, Santa Clara, CA
Chair: Tony Montalvo, Analog Devices Inc, Raleigh, NC

The scaling of CMOS analog and RF circuits traditionally lag that of digital design by one to two technology nodes. Today, the bulk of CMOS RF products are still in 0.13 - 0.18µm CMOS technology. However, the momentum towards increasing integration level of system-on-a-chip will lead RF designers, willingly or unwillingly, to follow their digital counterparts to 90nm and beyond. Several 90nm CMOS RF publications, admittedly research in nature, have appeared at recent ISSCC conferences. The trend should continue to 65nm, and, dare we say, 45nm and beyond. Besides the technical challenges of 90nm, the economic issues associated with deep submicron scaling can be equally daunting. The staggering mask cost, and long turn-times can create project management nightmares. How do we succeed in RF design at 90nm and beyond?

In this Special Topic Session, experts from academia and industry will describe some of the challenges that faces RF designers as we embrace the inevitable prediction of Moore's Law. They will address the advantages and obstacles to implementing CMOS RF circuits in deep submicron technology.

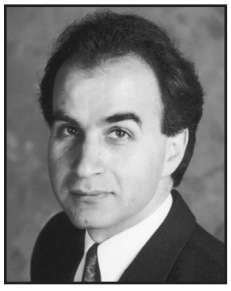
What are the characteristics of these technology and their impact to RF design. Does it make sense to simply port existing RF designs into 90nm or is it necessary/desirable to use a completely different approach? What are the economic issues related to nm technology? How do you deal with multi-million dollar mask sets? Does the presence of the RF on the same chip as the DSP slow the migration to the next, more advanced, technology? The speakers will address the technology characteristics, modeling issues, circuit design challenges, and a case study. This session promising to be enlightening and educational!

Position Statements



Technology Property Exploration for Analog/RF Design in 90nm and Beyond
Maarten Vertregt, Philips Research Labs, Eindhoven, Netherlands
Modern technology forces designers to reconsider the trade-offs between reduced precision and more, faster transistors. Advanced products (e.g. high-definition digital television and personal communication devices) demand highly-integrated systems-on-silicon, blending high-density digital functions with analog interface circuits. Those systems have to cope with high data-rates, and thus require high-performance (speed, dynamic range), without compromising power consumption. The combination of reduced device precision and increased performance demands novel choices on circuit and system level. Implications of technology scaling for the device properties relevant to circuit design will be explored. Furthermore, the various aspects of precision will be discussed, as well as ways in which designers can cope with those aspects on circuit level. The impact of deep sub-micron scaling on device properties and the subsequent evolution in analog and RF circuit topologies and performance will be explored.

RF Modeling Challenges at Deep Submicron CMOS
Sally Liu, TSMC, Hsin-chu, Taiwan
RF modeling is uniquely challenging in its own right in term of active devices, passives, interconnect and substrates. Recent trends of integrating RF functional blocks to a single SoC chip not only accelerate the schedule of nanometer RF modeling but also impose additional modeling challenges that are required to address design's concerns of performance, reliability, and cost. The ever-pronouncing leakage currents accentuate concerns on standby power and noise characteristics. Furthermore, the behaviors of these nanometer devices tuned for RF performance can be influenced even by its layout proximity. How would these nanometer effects impact the device behaviors and matching properties in RF applications? As we look forward in advances of compact modeling, the next generation models should measure up for both narrow band and wide band RF applications.



RF Design Challenges in Deep Submicron CMOS
Behzad Razavi, UCLA, Los Angeles, California
Since most RF systems are eventually integrated along with their digital baseband processor on the same chip, and since the RF section is typically much smaller in area than the digital section, the migration to finer technology nodes is likely to continue. The principal challenge in deep submicron design is, not surprisingly, the low supply voltage, as manifested in mixers, VCOs, frequency dividers, variable-gain stages, and power amplifiers (and LNAs if a broad bandwidth must be accommodated).

Other issues plaguing the design include the rapidly falling output impedance of the transistors and its nonlinearity, the gate leakage current (and its associated noise), and the problem of stress-induced mismatches. Of course, the higher transistor ft's and the larger number of metal levels (and hence slightly better inductors) serve as the redeeming features of these technologies and can be exploited to reduce the power dissipation and/or area.

Case Study on Single Chip Integration for Wireless
Bill Krenik, Texas Instruments Inc, Dallas, Texas
In December 2004, Texas Instruments sampled the world's first fully integrated GSM cellular phone IC. The device includes digital base band electronics, SRAM, the RF transceiver, power management, and analog circuitry, all integrated in 90nm CMOS. Fully integrated devices for GSM, CDMA, GPS, WLAN, Bluetooth, and DVB-H have also been announced by Texas Instruments and other companies. This presentation explains the motivation, methodology, business case, and technical results of the first GSM device as a case study. Single-chip integration of cell phone electronics is shown to offer substantial benefits in system board area, power consumption, and die area. Several key issues often associated with single-chip integration are examined. Critics' beware. This technology is real!!